

1 CLAIM LISTING

- 2 1. (Currently Amended) An apparatus for reducing the rate of temperature change in a
3 processing device due to a change in operational state for the processing device, the
4 apparatus including:
- 5 (a) a power transitioning arrangement for gradually transitioning power dissipation in
6 the processing device between a low power dissipation level and a high power
7 dissipation level in response to a change in a power state signal, the high power
8 dissipation level being relatively greater than the low power dissipation level;
- 9 (b) a cooling system alternatively providing a low thermal impedance for the
10 processing device and a relatively higher, high thermal impedance for the
11 processing device; and
- 12 (c) a cooling system controller for placing the cooling system at the high thermal
13 impedance in conjunction with a gradual transitioning from the high power
14 dissipation level to the low power dissipation level, and for placing the cooling
15 system at the low thermal impedance in conjunction with a gradual transitioning
16 from the low power dissipation level to the high power dissipation level.
- 17
- 18 2. (Original) The apparatus of Claim 1 wherein the power transitioning arrangement
19 includes a delay element for delaying the transitioning between power dissipation levels
20 relative to a change between the low thermal impedance and the high thermal impedance.
- 21
- 22 3. (Original) The apparatus of Claim 1 wherein the power transitioning arrangement
23 includes:

1 (a) a frequency divider connected to receive a system clock for the processing device
2 and having a frequency divider output; and

3 (b) a frequency controller operatively connected to the frequency divider for
4 controlling the frequency division function applied to the system clock by the
5 frequency divider.
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7 4. (Original) The apparatus of Claim 3 wherein the power transitioning arrangement further
8 includes a frequency divider bypass and a system clock output.
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10 5. (Original) The apparatus of Claim 3 further including a multiple clock distribution
11 system associated with the processing device for distributing both the system clock signal
12 and the frequency divider output to the processing device.
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14 6. (Original) The apparatus of Claim 1 wherein the power state signal comprises a
15 awake/sleep signal and the high power dissipation level corresponds to a maximum clock
16 rate for the processing device while the low power dissipation level corresponds to a
17 sleep clock rate for the processing device.
18

19 7. (Original) The apparatus of Claim 1 wherein the cooling system comprises a heat sink
20 and a fan positioned to affect airflow over the heat sink.
21

22 8. (Original) The apparatus of Claim 7 wherein the cooling system further includes a
23 cooling system switching device connected to receive the awake/asleep signal for the

1 processing device and a power on/off signal for a processing system including the
2 processing device.

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4 9. (Original) The apparatus of Claim 1 further including a power transitioning bypass
5 arrangement for causing the processing device to operate at the high power dissipation
6 level substantially immediately upon receipt of a power transitioning bypass signal.

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8 10. (Currently Amended) A processing system having at least one processing element
9 adapted to operate using a clock input, and also having a system power management
10 arrangement providing alternatively a high power state signal and a low power state
11 signal, the processing system including:

12 (a) a system clock arrangement providing the clock input to the processing system,
13 the system clock arrangement for gradually transitioning between power states by
14 transitioning from a high clock rate at the clock input to a relatively slower, low
15 clock rate at the clock input in response to a change from the high power state
16 signal to the low power state signal, the system clock arrangement also for
17 transitioning from the low clock rate at the clock input to the high clock rate in
18 response to a change from the low power state signal to the high power state
19 signal;

20 (b) a cooling system providing alternate thermal impedance states for transferring
21 heat from the processing system, the thermal impedance states including a high
22 thermal impedance state and a relatively lower, low thermal impedance state; and

1 (c) a cooling system controller operably connected to the cooling system for changing
2 the thermal impedance state of the cooling system from the high thermal
3 impedance state to the low thermal impedance state in response to a change from
4 the low power state signal to the high power state signal, and for changing the
5 thermal impedance state of the cooling system from the low thermal impedance
6 state to the high thermal impedance state in response to a change from the high
7 power state signal to the low power state signal.
8

9 11. (Original) The apparatus of Claim 10 wherein the power transitioning arrangement
10 includes a delay element for delaying the transitioning between power dissipation levels
11 relative to a change between the low thermal impedance and the high thermal impedance.
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13 12. (Original) The apparatus of Claim 10 wherein the power transitioning arrangement
14 includes:

- 15 (a) a frequency divider connected to receive a system clock for the processing device
16 and having a frequency divider output; and
17 (b) a frequency controller operatively connected to the frequency divider for
18 controlling the frequency division function applied to the system clock by the
19 frequency divider.
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21

1 13. (Original) The apparatus of Claim 12 wherein:

2 (a) the processing system includes a second processing element and the system clock
3 arrangement further includes a frequency divider bypass and a system clock input
4 to the processing system; and.

5 (b) the processing system further includes a multiple clock distribution system for
6 distributing both the system clock signal and the frequency divider output to the
7 processing system.

8
9 14. (Original) The apparatus of Claim 1 wherein the cooling system comprises a heat sink
10 and a fan positioned to affect airflow over the heat sink.

11
12 15. (Original) The apparatus of Claim 7 wherein the cooling system further includes a
13 cooling system switching device connected to receive the awake/asleep signal for the
14 processing device and a power on/off signal for a processing system including the
15 processing device.

16
17 16. (Original) The apparatus of Claim 1 further including a power transitioning bypass
18 arrangement for causing the processing device to operate at the high power dissipation
19 level substantially immediately upon receipt of a power transitioning bypass signal.

- 1 17. (Currently Amended) A method for reducing the rate of temperature change in a
2 processing device as the processing device undergoes a change in operational state, the
3 method including the steps of:
- 4 (a) gradually transitioning power dissipation in the processing device between a low
5 power dissipation level and a high power dissipation level in response to a change
6 in a power state signal, the high power dissipation level being relatively greater
7 than the low power dissipation level; and
- 8 (b) placing a cooling system for the processing device at a high thermal impedance in
9 conjunction with a gradual transitioning from the high power dissipation level to
10 the low power dissipation level, and placing the cooling system at the low thermal
11 impedance in conjunction with a gradual transitioning from the low power
12 dissipation level to the high power dissipation level.
- 13
- 14 18. (Original) The method of Claim 17 further including the step of delaying the
15 transitioning between power dissipation levels relative to a change between the low
16 thermal impedance and the high thermal impedance.
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- 18 19. (Original) The method of Claim 17 wherein the step of transitioning power dissipation
19 includes gradually modifying the clock rate of the processing device.
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1 20. (Currently Amended) The method of Claim [20] 17 wherein the step of transitioning
2 power dissipation includes modifying the power dissipation of different processing
3 elements in the processing device at different times.